UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/787,218	03/15/2001	Takuya Ishida	108107	6469

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EXAMINER
CLEARY, THOMAS J

ART UNIT	PAPER NUMBER
2111	15

DATE MAILED: 05/17/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

-- *The MAILING DATE of this communication appears on the cover sheet with the correspondence address* --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) FROM
THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed
  after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
  Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any
  earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on *25 February 2004*.
2a)☒ This action is **FINAL**.   2b)☐ This action is non-final.
3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is
closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-5 and 7-30* is/are pending in the application.
    4a) Of the above claim(s) _____ is/are withdrawn from consideration.
5)☒ Claim(s) *23,24 and 28-30* is/are allowed.
6)☒ Claim(s) *1,3-5,7-10,14-22 and 25-27* is/are rejected.
7)☒ Claim(s) *11-13* is/are objected to.
8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.
10)☒ The drawing(s) filed on *25 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.
    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
    a)☒ All b)☐ Some * c)☐ None of:
      1.☐ Certified copies of the priority documents have been received.
      2.☐ Certified copies of the priority documents have been received in Application No. _____.
      3.☒ Copies of the certified copies of the priority documents have been received in this National Stage
        application from the International Bureau (PCT Rule 17.2(a)).
    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
    Paper No(s)/Mail Date _____.

4) ☒ Interview Summary (PTO-413)
    Paper No(s)/Mail Date. *15* .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

	Application No.	Applicant(s)
Interview Summary	09/787,218	ISHIDA ET AL.
	Examiner	Art Unit	
	Thomas J. Cleary	2111	

All participants (applicant, applicant's representative, PTO personnel):

(1) *Thomas J. Cleary - USPTO*.

(3)*Daniel Tanner - 54734*.

(2) *Mark Rinehart - USPTO*.

(4)_____.

Date of Interview: *11-12 May 2004*.

Type: a)☒ Telephonic b)☐ Video Conference
    c)☐ Personal [copy given to: 1)☐ applicant   2)☐ applicant's representative]

Exhibit shown or demonstration conducted: d)☐ Yes   e)☒ No.
   If Yes, brief description: _____.

Claim(s) discussed: *1,5,9,23-25 and 28-30*.

Identification of prior art discussed: *N/A*.

Agreement with respect to the claims f)☐ was reached. g)☐ was not reached. h)☒ N/A.

Substance of Interview including description of the general nature of what was agreed to if an agreement was reached, or any other comments: *See Continuation Sheet*.

(A fuller description, if necessary, and a copy of the amendments which the examiner agreed would render the claims allowable, if available, must be attached. Also, where no copy of the amendments that would render the claims allowable is available, a summary thereof must be attached.)

THE FORMAL WRITTEN REPLY TO THE LAST OFFICE ACTION MUST INCLUDE THE SUBSTANCE OF THE INTERVIEW. (See MPEP Section 713.04). If a reply to the last Office action has already been filed, APPLICANT IS GIVEN ONE MONTH FROM THIS INTERVIEW DATE, OR THE MAILING DATE OF THIS INTERVIEW SUMMARY FORM, WHICHEVER IS LATER, TO FILE A STATEMENT OF THE SUBSTANCE OF THE INTERVIEW. See Summary of Record of Interview requirements on reverse side or on attached sheet.

Examiner Note: You must sign this form unless it is an
Attachment to a signed Office action.

_____
Examiner's signature, if required

Summary of Record of Interview Requirements

Manual of Patent Examining Procedure (MPEP), Section 713.04, Substance of Interview Must be Made of Record
A complete written statement as to the substance of any face-to-face, video conference, or telephone interview with regard to an application must be made of record in the application whether or not an agreement with the examiner was reached at the interview.

Title 37 Code of Federal Regulations (CFR) § 1.133 Interviews
Paragraph (b)
In every instance where reconsideration is requested in view of an interview with an examiner, a complete written statement of the reasons presented at the interview as warranting favorable action must be filed by the applicant. An interview does not remove the necessity for reply to Office action as specified in §§ 1.111, 1.135. (35 U.S.C. 132)

37 CFR §1.2 Business to be transacted in writing.
All business with the Patent or Trademark Office should be transacted in writing. The personal attendance of applicants or their attorneys or agents at the Patent and Trademark Office is unnecessary. The action of the Patent and Trademark Office will be based exclusively on the written record in the Office. No attention will be paid to any alleged oral promise, stipulation, or understanding in relation to which there is disagreement or doubt.

The action of the Patent and Trademark Office cannot be based exclusively on the written record in the Office if that record is itself incomplete through the failure to record the substance of interviews.

It is the responsibility of the applicant or the attorney or agent to make the substance of an interview of record in the application file, unless the examiner indicates he or she will do so. It is the examiner's responsibility to see that such a record is made and to correct material inaccuracies which bear directly on the question of patentability.

Examiners must complete an Interview Summary Form for each interview held where a matter of substance has been discussed during the interview by checking the appropriate boxes and filling in the blanks. Discussions regarding only procedural matters, directed solely to restriction requirements for which interview recordation is otherwise provided for in Section 812.01 of the Manual of Patent Examining Procedure, or pointing out typographical errors or unreadable script in Office actions or the like, are excluded from the interview recordation procedures below. Where the substance of an interview is completely recorded in an Examiners Amendment, no separate Interview Summary Record is required.

The Interview Summary Form shall be given an appropriate Paper No., placed in the right hand portion of the file, and listed on the "Contents" section of the file wrapper. In a personal interview, a duplicate of the Form is given to the applicant (or attorney or agent) at the conclusion of the interview. In the case of a telephone or video-conference interview, the copy is mailed to the applicant's correspondence address either with or prior to the next official communication. If additional correspondence from the examiner is not likely before an allowance or if other circumstances dictate, the Form should be mailed promptly after the interview rather than with the next official communication.

The Form provides for recordation of the following information:
- Application Number (Series Code and Serial Number)
- Name of applicant
- Name of examiner
- Date of interview
- Type of interview (telephonic, video-conference, or personal)
- Name of participant(s) (applicant, attorney or agent, examiner, other PTO personnel, etc.)
- An indication whether or not an exhibit was shown or a demonstration conducted
- An identification of the specific prior art discussed
- An indication whether an agreement was reached and if so, a description of the general nature of the agreement (may be by attachment of a copy of amendments or claims agreed as being allowable). Note: Agreement as to allowability is tentative and does not restrict further action by the examiner to the contrary.
- The signature of the examiner who conducted the interview (if Form is not an attachment to a signed Office action)

It is desirable that the examiner orally remind the applicant of his or her obligation to record the substance of the interview of each case. It should be noted, however, that the Interview Summary Form will not normally be considered a complete and proper recordation of the interview unless it includes, or is supplemented by the applicant or the examiner to include, all of the applicable items required below concerning the substance of the interview.

A complete and proper recordation of the substance of any interview should include at least the following applicable items:
1) A brief description of the nature of any exhibit shown or any demonstration conducted,
2) an identification of the claims discussed,
3) an identification of the specific prior art discussed,
4) an identification of the principal proposed amendments of a substantive nature discussed, unless these are already described on the Interview Summary Form completed by the Examiner,
5) a brief identification of the general thrust of the principal arguments presented to the examiner,
   (The identification of arguments need not be lengthy or elaborate. A verbatim or highly detailed description of the arguments is not required. The identification of the arguments is sufficient if the general nature or thrust of the principal arguments made to the examiner can be understood in the context of the application file. Of course, the applicant may desire to emphasize and fully describe those arguments which he or she feels were or might be persuasive to the examiner.)
6) a general indication of any other pertinent matters discussed, and
7) if appropriate, the general results or outcome of the interview unless already described in the Interview Summary Form completed by the examiner.

Examiners are expected to carefully review the applicant's record of the substance of an interview. If the record is not complete and accurate, the examiner will give the applicant an extendable one month time period to correct the record.

Examiner to Check for Accuracy

If the claims are allowable for other reasons of record, the examiner should send a letter setting forth the examiner's version of the statement attributed to him or her. If the record is complete and accurate, the examiner should place the indication, "Interview Record OK" on the paper recording the substance of the interview along with the date and the examiner's initials.

Continuation of Substance of Interview including description of the general nature of what was agreed to if an agreement was reached, or any other comments: Examiner initiated interview for clarification to insure compliance with Rule 83a. Applicant confirmed compliance with Rule 83a by indicating exemplary locations in the figures showing the elements claimed as follows: link circuit - Figure 4 Number 20; write circuit - Figure 4 Number 44; packet division circuit - Figure 4 Numbers 84 and 86 and Figure 19 Number 180; packet storage memory - Figure 4 Number 80; first bus for connecting to an application layer device - Figure 4 Number 90; second bus for controlling the data transfer control device - Figure 4 Number 95; third bus for connecting to a physical layer device - Figure 4 Number 100; fourth bus for connecting to the packet storage memory - Figure 4 Number 110; fifth bus for connecting to a circuit which implements part of the first layer protocol by hardware - Figure 4 Number 99; arbitration circuit which performs the arbitration for extablishing a data path between one of the first, second, third, and fifth buses and the fourth bus - Figure 4 Number 74, tag generation circuit - Figure 19 Number 162. Applicant further indicated that the claimed elements are fully disclosed in the specification and may appear at other locations in the drawings.

DETAILED ACTION

Drawings

1.   The drawings were received on 25 February 2004. These drawings are

acceptable.

Claim Rejections - 35 USC § 103

2.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set
> forth in section 102 of this title, if the differences between the subject matter sought to be patented and
> the prior art are such that the subject matter as a whole would have been obvious at the time the
> invention was made to a person having ordinary skill in the art to which said subject matter pertains.
> Patentability shall not be negatived by the manner in which the invention was made.

3.   Claims 1, 9, 14, 16, 17, 19, 20, 22, 25, 26, and 27 are rejected under 35 U.S.C.

103(a) as being unpatentable over US Patent Number 6,363,428 to Chou et al. ("Chou")

in view of US Patent Number 6,510,156 to Brock et al. ("Brock").

4.   In reference to Claim 1, Chou teaches a data transfer control device for

transferring data between a plurality of nodes connected to a bus, the data transfer

control device comprising: a link circuit which provides services for packet transfer

between nodes (See Figure 2 and Column 6 Lines 49-60); a write circuit which writes a

packet that has been received through the link circuit to a randomly accessible packet

storage memory (See Figure 2 and Column 3 Lines 47-52); and a packet division circuit

which writes first data of the packet for a first layer to a first data area of the packet

storage memory (See Column 3 Lines 8-19, Column 4 Lines 24-33, and Column 6 Lines

4-6), and writes second data of the packet for a second layer that is a layer above the

first layer to a second data area of the packet storage memory (See Column 3 Lines 20-

30, Column 4 Lines 35-39, and Column 6 Lines 4-6), wherein the first data is command

data used by the protocol of the first layer and the second data is data used by an

application layer (See Figure 3 and Column 2 Lines 40-49), and the second data is read

sequentially from the second data area and the read second data is transferred to an

application layer device (See Column 10 Lines 18-24). Because the content data is

audio/visual data, it is inherently read sequentially from the second data area. Chou

uses the method, known in the art, of packet encapsulation. Chou teaches placing a

packet conforming to the CIP Transport Protocol inside the data area of an IEEE-1394

packet. The packet of Chou thus consists of an IEEE-1394 packet header (equivalent

to the control information) (See Figure 3 '1394 Header') and an IEEE-1394 data area,

which consists of the CIP header (equivalent to the command data used by the protocol

of the first header) (See Figure 3 'Protocol Header') and the CIP data (equivalent to the

data used by an application layer) (See Figure 3 'AV Content Data'). Chou further

describes packet encapsulation in Column 2 Lines 29-49. Chou does not teach that the

packet division circuit writes control information of the packet to a control information

area of the packet storage memory. Brock teaches saving the header of a packet to

memory (See Column 4 Lines 45-60).

It would have been obvious to one of ordinary skill in the art at the time the

invention was made to combine the device of Chou with the ability to save the header of

a packet of Brock, resulting in the invention of Claim 1, in order to allow subsequent

packets that have the same header as a previously sent packet to be sent payload only

(See Column 4 Lines 52-58 of Brock), thus improving the efficiency and speed of the

device.

5.   In reference to Claim 9, Chou teaches a data transfer control device for

transferring data between a plurality of nodes connected to a bus, the data transfer

control device comprising: a link circuit which provides services for packet transfer

between nodes (See Figure 2 and Column 6 Lines 49-60); a write circuit which writes a

packet that has been received through the link circuit to a randomly accessible packet

storage memory (See Figure 2 and Column 3 Lines 47-52); a circuit which reads the

packet that has been written to the packet storage memory and transfers the packet to

the link circuit (See Column 10 Lines 21-24); and that the packet storage memory has a

data area in which is stored packet data, and the data area is divided into a first data

area for storing first data from a first layer (See Column 3 Lines 8-19, Column 4 Lines

24-33, and Column 6 Lines 4-6) and a second data area for storing second data for a

second layer (See Column 3 Lines 20-30, Column 4 Lines 35-39, and Column 6 Lines

4-6); wherein the first data is command data used by the protocol of the first layer and

the second data is data used by an application layer (See Figure 3 and Column 2 Lines

40-49), and the second data is read sequentially from the second data area and the

read second data is transferred to an application layer device (See Column 10 Lines 18-

24). Because the content data is audio/visual data, it is inherently read sequentially

from the second data area. Chou uses the method, known in the art, of packet

encapsulation. Chou teaches placing a packet conforming to the CIP Transport

Protocol inside the data area of an IEEE-1394 packet. The packet of Chou thus

consists of an IEEE-1394 packet header (equivalent to the control information) (See

Figure 3 '1394 Header') and an IEEE-1394 data area, which consists of the CIP header

(equivalent to the command data used by the protocol of the first header) (See Figure 3

'Protocol Header') and the CIP data (equivalent to the data used by an application layer)

(See Figure 3 'AV Content Data'). Chou further describes packet encapsulation in

Column 2 Lines 29-49. Chou does not teach that the packet division circuit writes

control information of the packet to a control information area of the packet storage

memory. Brock teaches saving the header of a packet to memory (See Column 4 Lines

45-60).

It would have been obvious to one of ordinary skill in the art at the time the

invention was made to combine the device of Chou with the ability to save the header of

a packet of Brock, resulting in the invention of Claim 9, in order to allow subsequent

packets that have the same header as a previously sent packet to be sent payload only

(See Column 4 Lines 52-58 of Brock), thus improving the efficiency and speed of the

device.

6.   In reference to Claim 14, Chou and Brock teach the limitations as applied to

Claim 1 above. Chou further teaches that the data transfer is in accordance with the

IEEE 1394 standard (See Figure 2 and Column 2 Line 63 – Column 3 Line 7).

It would have been obvious to one of ordinary skill in the art at the time the

invention was made to combine the device of Chou with the ability to save the header of

a packet of Brock, resulting in the invention of Claim 14, in order to allow subsequent

packets that have the same header as a previously sent packet to be sent payload only

(See Column 4 Lines 52-58 of Brock), thus improving the efficiency and speed of the

device.

7.   In reference to Claim 16, Chou and Brock teach the limitations as applied to

Claim 9 above. Chou further teaches that the data transfer is in accordance with the

IEEE 1394 standard (See Figure 2 and Column 2 Line 63 – Column 3 Line 7).

It would have been obvious to one of ordinary skill in the art at the time the

invention was made to combine the device of Chou with the ability to save the header of

a packet of Brock, resulting in the invention of Claim 16, in order to allow subsequent

packets that have the same header as a previously sent packet to be sent payload only

(See Column 4 Lines 52-58 of Brock), thus improving the efficiency and speed of the

device.

8.   In reference to Claim 17, Chou and Brock teach the limitations as applied to

Claim 1 above. Chou further teaches a device which performs given processing on

data that has been received from another node through the data transfer control device

and a bus (See Figure 2 Number 20, Column 6 Line 66 – Column 7 Line 2, and Column

10 Lines 21-24); and a device which outputs or stores data that has been subjected to

processing (See Figure 2 Numbers 12, 22, 30, and 32, Column 6 Lines 61-66, and

Column 7 Lines 3-17).

It would have been obvious to one of ordinary skill in the art at the time the

invention was made to combine the device of Chou with the ability to save the header of

a packet of Brock, resulting in the invention of Claim 17, in order to allow subsequent

packets that have the same header as a previously sent packet to be sent payload only

(See Column 4 Lines 52-58 of Brock), thus improving the efficiency and speed of the

device.

9.   In reference to Claim 19, Chou and Brock teach the limitations as applied to

Claim 9 above. Chou further teaches a device which performs given processing on

data that has been received from another node through the data transfer control device

and a bus (See Figure 2 Number 20, Column 6 Line 66 – Column 7 Line 2, and Column

10 Lines 21-24); and a device which outputs or stores data that has been subjected to

processing (See Figure 2 Numbers 12, 22, 30, and 32, Column 6 Lines 61-66, and

Column 7 Lines 3-17).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Chou with the ability to save the header of a packet of Brock, resulting in the invention of Claim 19, in order to allow subsequent packets that have the same header as a previously sent packet to be sent payload only (See Column 4 Lines 52-58 of Brock), thus improving the efficiency and speed of the device.

10.   In reference to Claim 20, Chou and Brock teach the limitations as applied to Claim 1 above. Chou further teaches that the CPU can take in data to be subject to processing (See Figure 2 Number 20 and Column 10 Lines 21-24). Since the internal bus is bidirectional (See Figure 2 and Column 6 Lines 47-48), and since the interface circuitry can both send and receive data (See Figure 2 and Column 6 Lines 49-60), it is inherent that the CPU can perform processing on data that is to be transferred to another node through the interface circuit and the bus. Chou further teaches that data to be subjected to processing can be taken in through a keyboard, a mouse, or the 1394 link (See Figure 2 and Column 7 Lines 3-10).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Chou with the ability to save the header of a packet of Brock, resulting in the invention of Claim 20, in order to allow subsequent packets that have the same header as a previously sent packet to be sent payload only (See Column 4 Lines 52-58 of Brock), thus improving the efficiency and speed of the device.

11.   In reference to Claim 22, Chou and Brock teach the limitations as applied to

Claim 9 above. Chou further teaches that the CPU can take in data to be subject to

processing (See Figure 2 Number 20 and Column 10 Lines 21-24). Since the internal

bus is bidirectional (See Figure 2 and Column 6 Lines 47-48), and since the interface

circuitry can both send and receive data (See Figure 2 and Column 6 Lines 49-60), it is

inherent that the CPU can perform processing on data that is to be transferred to

another node through the interface circuit and the bus. Chou further teaches that data

to be subjected to processing can be taken in through a keyboard, a mouse, or the 1394

link (See Figure 2 and Column 7 Lines 3-10).

It would have been obvious to one of ordinary skill in the art at the time the

invention was made to combine the device of Chou with the ability to save the header of

a packet of Brock, resulting in the invention of Claim 22, in order to allow subsequent

packets that have the same header as a previously sent packet to be sent payload only

(See Column 4 Lines 52-58 of Brock), thus improving the efficiency and speed of the

device.

12.   In reference to Claim 25, Chou and Brock teach the limitations as applied to

Claim 1 above. Chou further teaches a unit for maintaining an address for storing each

data portion, which is equivalent to a tag generation circuit which generates a tag being

information for delimiting writing areas (See Column 3 Lines 30-33).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Chou with the ability to save the header of a packet of Brock, resulting in the invention of Claim 25, in order to allow subsequent packets that have the same header as a previously sent packet to be sent payload only (See Column 4 Lines 52-58 of Brock), thus improving the efficiency and speed of the device.

13.   In reference to Claim 26, Chou and Brock teach the limitations as applied to Claim 1 above. The CIP header of Chou, which functions in the same manner as an operational request block and is responsible for controlling the CIP content field (See Figure 3 and Column 2 Lines 29-49), is equivalent to an operational request block (ORB) area. The CIP data area containing audio/visual data, which is received as a stream isochronously (See Figure 3 and Column 2 Lines 29-49) is equivalent to a stream area.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Chou with the ability to save the header of a packet of Brock, resulting in the invention of Claim 26, in order to allow subsequent packets that have the same header as a previously sent packet to be sent payload only (See Column 4 Lines 52-58 of Brock), thus improving the efficiency and speed of the device.

14.   In reference to Claim 27, Chou and Brock teach the limitations as applied to

Claim 9 above. The CIP header of Chou, which functions in the same manner as an

operational request block and is responsible for controlling the CIP content field (See

Figure 3 and Column 2 Lines 29-49), is equivalent to an operational request block

(ORB) area. The CIP data area containing audio/visual data, which as a stream

isochronously (See Figure 3 and Column 2 Lines 29-49) is equivalent to a stream area.

It would have been obvious to one of ordinary skill in the art at the time the

invention was made to combine the device of Chou with the ability to save the header of

a packet of Brock, resulting in the invention of Claim 27, in order to allow subsequent

packets that have the same header as a previously sent packet to be sent payload only

(See Column 4 Lines 52-58 of Brock), thus improving the efficiency and speed of the

device.

15.   Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chou and

Brock as applied to Claim 1 above, and further in view of English Language Abstract of

Japanese Patent Application Publication 06069913 to Nakamura et al. ("Nakamura").

16.   In reference to Claim 3, Chou and Brock teach the limitations as applied to Claim

1 above. Chou and Brock do not teach the data transfer control device further

comprising area management circuit which makes a full signal go active when the

second data area is full, to inhibit the write circuit from writing the second data to the

second data area, and makes and empty signal go active when the second data area is

empty, to inhibit the second layer from reading the second data from the second data

area. Nakamura teaches a device that counts packets read from and written to a

memory, and inhibits reading transmission data from the memory when the memory is

empty and inhibits writing reception data to the memory when the memory is full (See

Abstract of Nakamura).

It would have been obvious to one of ordinary skill in the art at the time the

invention was made to combine the device of Chou and Brock with the device of

Nakamura, resulting in the invention of Claim 3, in order to accurately implement packet

data reads and writes to and from memory (See Abstract of Nakamura).

17.   Claims 4, 5, 7, 8, 15, 18, and 21 are rejected under 35 U.S.C. 103(a) as being

unpatentable over Chou and Brock as applied to Claim 1 above, and further in view of

US Patent Number 6,115,770 to Gehman ("Gehman"), US Patent Number 6,272,114 to

Kobayashi ("Kobayashi"), and US Patent Number 6,351,783 to Garney et al. ("Garney").

18.   In reference to Claim 4, Chou and Brock teach the limitations as applied to Claim

1 above. Chou and Brock do not teach a request packet which is used for starting a

transaction being transmitted to a responding node, transaction identification

information comprised within the request packet including indication information which

indicates processing to be performed when a response packet from the responding

node is received, and the control information and the first and second data of the

response packet being written into an separate data areas specified by the indication

information within the transaction identification information of the response packet when

the response packet from the responding node is received. Gehman teaches that data

can be obtained from a node by sending a read request packet, according to the IEEE

1394 Standard, which contains a tcode field. The node then responds by packetizing

the data according to the 1394 Standard and sends it to the requesting node. The

response packet contains information regarding the destination address for the data at

the destination node (See Column 5 Lines 30-55 of Gehman). Kobayashi teaches that

the tcode field of a 1394 Standard packet can provide information about the process to

be executed (See Figure 7 and Column 5 Lines 35-42 of Kobayashi). Garney teaches

an isochronous write packet having transaction information indicating the destination in

memory to which data is to be stored (See Column 3 Lines 39-41). The packet of Chou

is equivalent to the request and response packets of Claim 4 and functions in an

equivalent matter.

It would have been obvious to one of ordinary skill in the art at the time the

invention was made to combine the device of Chou and Brock with the packet

communication formats of Gehman, Kobayashi, and Garney, resulting in the invention

of Claim 4, in order to provide a means for a device to access a bus management

register across a 1394 link (See Column 5 Lines 30-33 of Gehman), and to provide and

indication of where to store or retrieve data from memory (See Column 3 Lines 37-42 of

Garney).

19.   In reference to Claim 5, Chou teaches a circuit that performs the processing

indicated by the identification information of the response packet when the response

packet of the responding node is received (See Figure 2, Column 6 Lines 43-48, and

Column 7 Lines 3-10 of Chou). Chou does not teach a circuit that makes transaction

identification information within a request packet include indication information that

indicates processing to be performed after reception of a response packet from a

responding node when the request packet that is used for starting a transaction is

transmitted to the responding node and the control information and the first and second

data of the response packet being written into an separate data areas specified by the

indication information within the transaction identification information of the response

packet when the response packet from the responding node is received. Gehman

teaches that data can be obtained from a node by sending a read request packet,

according to the IEEE 1394 Standard, which contains a tcode field. The node then

responds by packetizing the data according to the 1394 Standard and sends it to the

requesting node (See Column 5 Lines 30-55 of Gehman). Kobayashi teaches that the

tcode field of a 1394 Standard packet can provide information about the process to be

executed (See Figure 7 and Column 5 Lines 35-42 of Kobayashi). Garney teaches an

isochronous write packet having transaction information indicating the destination in

memory to which data is to be stored (See Column 3 Lines 39-41). The packet of Chou

is equivalent to the request and response packets of Claim 5 and functions in an

equivalent matter.

It would have been obvious to one of ordinary skill in the art at the time the

invention was made to combine the device of Chou and Brock with the packet

communication formats of Gehman, Kobayashi, and Garney, resulting in the invention

of Claim 5, in order to provide a means for a device to access a bus management

register across a 1394 link (See Column 5 Lines 30-33 of Gehman), and to provide and

indication of where to store or retrieve data from memory (See Column 3 Lines 37-42 of

Garney).

20.   In reference to Claim 7, Chou, Brock, Gehman, Kobayashi, and Garney teach the

limitations as applied to Claim 5 above. Kobayashi inherently teaches that a bit of the

tcode is reserved for expressing the processing to be performed, which is equivalent to

the identification information (See Column 5 Liens 35-42).

It would have been obvious to one of ordinary skill in the art at the time the

invention was made to combine the device of Chou and Brock with the packet

communication formats of Gehman, Kobayashi, and Garney, resulting in the invention

of Claim 7, in order to provide a means for a device to access a bus management

register across a 1394 link (See Column 5 Lines 30-33 of Gehman), and to provide and

indication of where to store or retrieve data from memory (See Column 3 Lines 37-42 of

Garney).

21.   In reference to Claim 8, Chou, Brock, Gehman, Kobayashi, and Garney teach the

limitations as applied to Claim 5 above. Chou further teaches that the data transfer is in

accordance with the IEEE 1394 standard, and thus the transaction identification

information is a transaction label in accordance with said standard (See Figure 2 and

Column 2 Line 63 – Column 3 Line 7).

It would have been obvious to one of ordinary skill in the art at the time the

invention was made to combine the device of Chou and Brock with the packet

communication formats of Gehman, Kobayashi, and Garney, resulting in the invention

of Claim 8, in order to provide a means for a device to access a bus management

register across a 1394 link (See Column 5 Lines 30-33 of Gehman), and to provide and

indication of where to store or retrieve data from memory (See Column 3 Lines 37-42 of

Garney).

22.   In reference to Claim 15, Chou, Brock, Gehman, Kobayashi, and Garney teach

the limitations as applied to Claim 5 above. Chou further teaches that the data transfer

is in accordance with the IEEE 1394 standard (See Figure 2 and Column 2 Line 63 –

Column 3 Line 7).

It would have been obvious to one of ordinary skill in the art at the time the

invention was made to combine the device of Chou and Brock with the packet

communication formats of Gehman, Kobayashi, and Garney, resulting in the invention

of Claim 15, in order to provide a means for a device to access a bus management

register across a 1394 link (See Column 5 Lines 30-33 of Gehman), and to provide and

indication of where to store or retrieve data from memory (See Column 3 Lines 37-42 of

Garney).

23.   In reference to Claim 18, Chou, Brock, Gehman, Kobayashi, and Garney teach

the limitations as applied to Claim 5 above. Chou further teaches a device which

performs given processing on data that has been received from another node through

the data transfer control device and a bus (See Figure 2 Number 20, Column 6 Line 66

– Column 7 Line 2, and Column 10 Lines 21-24); and a device which outputs or stores

data that has been subjected to processing (See Figure 2 Numbers 12, 22, 30, and 32,

Column 6 Lines 61-66, and Column 7 Lines 3-17).

It would have been obvious to one of ordinary skill in the art at the time the

invention was made to combine the device of Chou and Brock with the packet

communication formats of Gehman, Kobayashi, and Garney, resulting in the invention

of Claim 18, in order to provide a means for a device to access a bus management

register across a 1394 link (See Column 5 Lines 30-33 of Gehman), and to provide and

indication of where to store or retrieve data from memory (See Column 3 Lines 37-42 of

Garney).

24.   In reference to Claim 21, Chou, Brock, Gehman, Kobayashi, and Garney teach

the limitations as applied to Claim 5 above. Chou further teaches that the CPU can take

in data to be subject to processing (See Figure 2 Number 20 and Column 10 Lines 21-

24). Since the internal bus is bidirectional (See Figure 2 and Column 6 Lines 47-48),

and since the interface circuitry can both send and receive data (See Figure 2 and

Column 6 Lines 49-60), it is inherent that the CPU can perform processing on data that

is to be transferred to another node through the interface circuit and the bus. Chou

further teaches that data to be subjected to processing can be taken in through a

keyboard, a mouse, or the 1394 link (See Figure 2 and Column 7 Lines 3-10).

It would have been obvious to one of ordinary skill in the art at the time the

invention was made to combine the device of Chou and Brock with the packet

communication formats of Gehman, Kobayashi, and Garney, resulting in the invention

of Claim 21, in order to provide a means for a device to access a bus management

register across a 1394 link (See Column 5 Lines 30-33 of Gehman), and to provide and

indication of where to store or retrieve data from memory (See Column 3 Lines 37-42 of

Garney).

25.   Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chou

and Brock as applied to Claim 9 above, and further in view of English Language

Abstract of Japanese Patent Number 358101544 to Nishijima ("Nishijima") and US

Patent Number 6,385,113 to Longwell et al. ("Longwell").

26.   In reference to Claim 10, Chou and Brock teach the limitations as applied to

Claim 9 above. Chou and Brock do not teach a first address storage register which

stores a transmission area start address for reserving a transmission area in the second

data area, a second address storage register which stores a transmission area end

address for reserving a transmission area in the second data area, a third address

storage register which stores a reception area start address for reserving a reception

area in the second data area, and a fourth address storage register which stores a

reception area end address for reserving a reception area in the second data area.

Nishijima teaches a memory area that is divided into a transmission area and a

reception area (See Abstract and Figures 5 and 6 of Nishijima). Longwell teaches

registers for storing a first start address, a second start address, a first address range

(equivalent to the first end address of Claim 10), and a second address range

(equivalent to the second end address of Claim 10) (See Figure 16 and Column 14

Lines 17-28 of Longwell).

It would have been obvious to one of ordinary skill in the art at the time the

invention was made to combine the device of Chou and Brock with the memory having

transmission and reception areas of Nishijima and the registers of Longwell, resulting in

the invention of Claim 10, in order to keep the transmission and reception areas

separate (See Figures 5 and 6 of Nishijima) and to provide the active or inactive status

of those areas of memory (See Column 14 Lines 17-19 of Longwell).

Response to Arguments

27.   Applicant's arguments with respect to Claims 1 and 9 have been fully considered

but are moot in view of the new ground(s) of rejection. Applicant has modified the

scope of the claims. As shown above, such changes are not persuasive to overcome a

rejection based on 35 USC §103. The new ground(s) of rejection presented in this

Office action in reference to the aforementioned claims have been necessitated by the

Applicant's amendment. The Examiner notes that Chou uses a method of packet

encapsulation in which a packet consists of a header and a data area wherein the data

area further consists of another packet consisting of a header and data area. These

three packet segments are stored in separate, contiguous memory areas as described

in the aforementioned rejections. Thus, the Examiner notes that the methods disclosed

in Chou more closely correspond to the example illustrated in Figure 10 of the present

application. Further, as shown in the aforementioned rejections, the amendments to the

claims have not further specified the type and functionality of the first and second data

to a degree which distinguishes it over the prior art.

28.   Applicant's arguments with respect to Claim 3 have been fully considered but are

moot in view of the new ground(s) of rejection. Applicant has modified the scope of the

claim. As shown above, such changes are not persuasive to overcome a rejection

based on 35 USC §103. The new ground(s) of rejection presented in this Office action

in reference to the aforementioned claims have been necessitated by the Applicant's

amendment.

29.   Applicant's arguments with respect to Claims 4, 5, 6, 8, 15, 18, and 21 have been

fully considered but are moot in view of the new ground(s) of rejection. Applicant has

modified the scope of the claims. As shown above, such changes are not persuasive to

overcome a rejection based on 35 USC §103. The new ground(s) of rejection

presented in this Office action in reference to the aforementioned claims have been

necessitated by the Applicant's amendment. As shown in the rejection of Claim 5, the

amendments to the claim have not further specified the type and functionality of the first

and second data to a degree which distinguishes it over the prior art.

30.   Applicant's arguments with respect to Claim 10 have been fully considered but

are moot in view of the new ground(s) of rejection. Applicant has modified the scope of

the claim. As shown above, such changes are not persuasive to overcome a rejection

based on 35 USC §103. The new ground(s) of rejection presented in this Office action

in reference to the aforementioned claims have been necessitated by the Applicant's

amendment.

Allowable Subject Matter

31.   Claims 11, 12, and 13 are objected to as being dependent upon a rejected base

claim, but would be allowable if rewritten in independent form including all of the

limitations of the base claim and any intervening claims.

32.   The following is a statement of reasons for the indication of allowable subject

matter: Claims 11, 12, and 13 would be allowable over the prior art of record if rewritten

in independent form because the Examiner found neither prior art cited in its entirety,

nor based on the prior art, found any motivation to combine any of the said prior art.

33.   In reference to Claim 11, prior art fails to teach the transmission area start

address and the reception area start address being set to the start address of the

second data area, and the transmission area end address and the reception area end

address being set to the end address of the second data area.

34.   In reference to Claim 12, prior art fails to teach both the transmission area start

address and the transmission area end address being set to either the start address or

the end address of the second data area, the reception area start address being set to

the start address of the second data area, and the reception area end address being set

to the end address of the second data area.

35.   In reference to Claim 13, prior art fails to teach both the reception area start

address and the reception area end address being set to either the start address or the

end address of the second data area, the transmission area start address being set to

the start address of the second data area, and the transmission area end address being

set to the end address of the second data area.

36.   Claims 23, 24, 28, 29, and 30 are allowed.

37.   The following is an examiner's statement of reasons for allowance: Claims 23,

24, 28, 29, and 30 are allowable over the prior art of record because the Examiner

found neither prior art cited in its entirety, nor based on the prior art, found any

motivation to combine any of the said prior art.

38.   In reference to Claim 23, prior art fails to teach a first bus for connecting to an

application layer device; a second bus for controlling the data transfer control device; a

third bus for connecting to a physical layer device; a fourth bus for connecting to the

packet storage memory; a fifth bus for connecting to a circuit which implements part of

the first layer protocol by hardware; and an arbitration circuit which performs the

arbitration for establishing a data path between one of the first second, third, and fifth

buses and the fourth bus.

39.   In reference to Claim 24, prior art fails to teach a first bus for connecting to an

application layer device; a second bus for controlling the data transfer control device; a

third bus for connecting to a physical layer device; a fourth bus for connecting to the

packet storage memory; a fifth bus for connecting to a circuit which implements part of

the first layer protocol by hardware; and an arbitration circuit which performs the

arbitration for establishing a data path between one of the first second, third, and fifth

buses and the fourth bus.

40.   In reference to Claim 28, prior art fails to teach the transmission area start

address and the reception area start address being set to the start address of the

second data area, and the transmission area end address and the reception area end

address being set to the end address of the second data area.

41.   In reference to Claim 29, prior art fails to teach both the transmission area start

address and the transmission area end address being set to either the start address or

the end address of the second data area, the reception area start address being set to

the start address of the second data area, and the reception area end address being set

to the end address of the second data area.

42.   In reference to Claim 30, prior art fails to teach both the reception area start

address and the reception area end address being set to either the start address or the

end address of the second data area, the transmission area start address being set to

the start address of the second data area, and the transmission area end address being

set to the end address of the second data area.

43.   Any comments considered necessary by applicant must be submitted no later

than the payment of the issue fee and, to avoid processing delays, should preferably

accompany the issue fee. Such submissions should be clearly labeled "Comments on

Statement of Reasons for Allowance."

Conclusion

44.   Applicant's amendment necessitated the new ground(s) of rejection presented in

this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP

§ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37

CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE

MONTHS from the mailing date of this action. In the event a first reply is filed within

TWO MONTHS of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the

shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later

than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Thomas J. Cleary whose telephone number is 703-305-

5824. The examiner can normally be reached on Monday-Thursday (7-4), Alt. Fridays
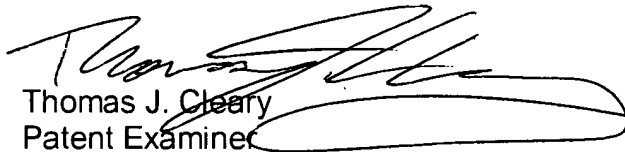
(7-3).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Mark H. Rinehart can be reached on 703-305-4815. The fax phone number ·

for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the

Patent Application Information Retrieval (PAIR) system. Status information for

published applications may be obtained from either Private PAIR or Public PAIR.

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you have questions on access to the Private PAIR system, contact the Electronic

Business Center (EBC) at 866-217-9197 (toll-free).

tjc

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